Remarks

This paper is in response to the Office Action dated Dec. 3, 2003. No claims have been amended in this response. Claims 6-16 and 21-31 are currently pending. Reexamination and reconsideration are respectfully requested.

Applicant thanks the Examiner for indicating that claims 16, 21-26 and 30 are allowed.

Claims 9-12 had previously been rejected under 35 U.S.C. 112. It appears that the rejection has been withdrawn. The Examiner did not discuss these claims in the discussion of the other claims rejected over the cited art. However, the Examiner did not state that the claims were allowed. Applicant respectfully submits that the Office Action is unclear as to the status of claims 9-12. Applicant respectfully submits that due to the apparent withdrawal of the section 112 rejection, claims 9-12 are in patentable form.

Applicant thanks the Examiner for the telephone interview held on Feb. 2, 2004. The proposed combination of references (US 5,181,090 to Maruo and US 4,637,128 to Mizutani) was discussed, including features relating to the layout of certain layers in the references. Final agreement was not reached. However, the Examiner indicated that he would consider additional comments (in this response) regarding deficiencies of the proposed combination of references.

Claims 6-7, 13-15 and 27 were rejected under 35 U.S.C. 103(a) as unpatentable over U.S. Patent No. 5,181,090 to Maruo ("Maruo") in combination with U.S. Patent No. 4,637,128 to Mizutani ("Mizutani"). The rejection is respectfully traversed.

Applicant respectfully submits that the Examiner has not met his burden to establish a suggestion or motivation in the art for the proposed combination and modification of the prior art. To establish a prima facie case of obviousness, there should be a suggestion or motivation in the art to modify the reference or to combine reference teachings, there should be a reasonable expectation of success, and the reference(s) must teach all the claim limitations. MPEP section 706.02(j). Applicant respectfully submits that the Examiner's citations to the art are insufficient to satisfy the criteria above.

The Examiner stated in the Office Action that the rejection was maintained as stated in the previous Office Action dated May 21, 2003. In the May 21, 2003 Office Action, the Examiner stated on page 4 that the combination "would enable formation of LOCOS oxide layers 11 and 15 of Maruo to be performed." However, applicant respectfully submits that one of

ordinary skill would not reasonably make the proposed combination.

The position and spacing of the various regions in Mizutani appears to differ substantially from those in Maruo as cited by the Examiner. For example, in Fig. 3(i) of Maruo (cited by the Examiner), the LOCOS layers 15 are positioned adjacent to the gate dielectric layer 14" under the gate electrode 14. The LOCOS layers 15 are also positioned directly above the offset impurity layers 17. A channel region extends between the offset impurity layers 17 under the gate electrode 16 and gate dielectric 14". The LOCOS oxide layers 11 in Maruo (Fig. 3(i)) are positioned over channel stopper regions 12, which are positioned outside of the source and drain regions 18 and 18a. Thus, the position of the layers in the substrate in well 13 includes a channel region in the substrate under the gate electrode 16, offset impurity layers 17 outside of the channel region, source and drain regions 18, 18a outside of the offset impurity layers 17, and channel stopper regions 12 outside of the source and drain regions 18, 18a. The LOCOS layers 15 are positioned directly over the offset impurity layers 17 and the LOCOS layers 11 are positioned directly over the channel stopper regions 12.

Mizutani, on the other hand, appears to teach a different position of the LOCOS layers relative to the gate electrode and the other layers. The substitution of the LOCOS layers of Mizutani for LOCOS layers 15 and 11 of Maruo would appear to yield a substantially different structure than Maruo.

For example, as seen in Mizutani Fig. 4H, LOCOS layers 60 are shown. The LOCOS layers 60 appear to be positioned further away from the gate electrode than in Maruo as cited by the Examiner. For example, Mizutani appears to show source and drain regions 70A and 70B directly outside of the channel region under the gate electrode 68, with low dose regions 64A and 64B outside of the source and drain regions and then high density regions 62 outside of the low density regions 64A and 64B. The LOCOS regions 60 are positioned outside of the source and drain regions 70A and 70B, whereas in Maruo Fig. 3(i), the LOCOS layers 15 are positioned inside of the source and drain regions 18 and 18a. In addition, Mizutani (Fig. 4H) positions the offset layer outside of the source and drain regions 70A and 70B, whereas Maruo (Fig. 3(i)) positions the offset layer inside of the source and drain regions 18 and 18a.

To form the LOCOS layers 15 and 11 of Maruo using the Mizutani process as cited by the Examiner would change the layout of the various layers, likely change the dimensions of the

device, and likely change the electrical properties of the device.

In addition to the features discussed above, it is noted that the LOCOS layers 15 and 11 in Maruo (Fig. 3(i)) appear to be formed to have different widths, with the inner LOCOS layers 15 being significantly less wide than the outer LOCOS layers 11. The Examiner cited no portion of Mizutani that describes forming different LOCOS layers to have differing widths.

The Examiner's citations to the art do not establish that one would desire to make the proposed combination and do not establish a reasonable likelihood of success for the proposed combination. As a result, applicant respectfully submits that the Examiner has not made out a prima facie case of obviousness and the rejection should be withdrawn.

Moreover, even if the references were combined, the combination suggested by the Examiner does not yield a method such as that recited in the claims. As seen, for example, in Mizutani Fig. 4H, what the Examiner appears to refer to as recessed sections in substrate 50 are spaced away from the gate region and appear to be positioned outside of the source and drain regions 70A and 70B. Applicant submits that the Examiner's citations to Mizutani do not describe or suggest that "a first semi-recessed LOCOS layer is provided between the gate dielectric layer and the drain region" and "a second semi-recessed LOCOS layer is provided between the gate dielectric layer and the source region" as recited in claim 6.

Thus, for at least the reasons stated above, applicant respectfully submits that the Examiner has not established a prima facie case of obviousness and accordingly, the rejection of claim 6 and its dependent claims 7 and 13-15 should be withdrawn. The rejection of claim 27 should also be withdrawn for at least reasons similar to those describe above for claim 6.

Moreover, claim 27 includes elements relating to multiple implantations. Applicant further notes that the Examiner's proposed combination does not appear to describe or suggest a method including at least the following steps:

> *forming a first recessed section in regions where the first semi-recessed LOCOS layer is to be formed, a second recessed section in regions where the second semi-recessed LOCOS layer is to be formed and a third recessed section in a region where the element isolation region is to be formed;*
>
> *performing a first implantation to implant ions into the semiconductor substrate in the first and second recessed sections and in end regions of the third recessed section;*

performing a second implantation to implant ions into the substrate at a central region of third recessed section;

as recited in claim 27. Accordingly, the rejection of claim 27 should also be withdrawn for this reason.

In view of the above, applicant respectfully submits that the Examiner's citations to the art: (1) do not provide an adequate a suggestion or motivation in the art to modify the reference or to combine reference teachings; (2) do not provide a reasonable expectation of success; and (3) do not teach all the claim limitations. A deficiency in any one of these criteria means that a prima facie case of obviousness has not been made out. Here, all three criteria are not met. Accordingly, applicant respectfully submits that the rejection should be withdrawn.

Claim 8 was also rejected under 35 U.S.C. 103(a) as being unpatentable over Maruo in view of Mizutani. The rejection is respectfully traversed. Claim 8 depends from claim 7 which depends from claim 6. Applicant respectfully submits that the rejection of claim 8 should be withdrawn for at least the same reasons as claim 6 as described above.

Claims 28-29 were rejected under 35 U.S.C. 103(a) as being unpatentable over Maruo in view of Mizutani, and further in view of U.S. Patent No. 6,423,631 to Iyer et al ("Iyer"). The rejection is respectfully traversed. Applicant respectfully submits that the rejection of claims 28-29 should be withdrawn for at least similar reasons as those discussed above for claim 6, and that the Examiner's citation to Iyer does not overcome the deficiencies of the combination of Maruo and Mizutani as described above.

Applicant notes that claim 31 does not appear to have been examined by the Examiner, as it is not mentioned in the Office Action. Claim 31 was added in the previous response (amendment) filed by applicant. Applicant respectfully requests that claim 31 be examined.

The Office Action also included various comments concerning the art and the non-patentability of features in various of the above mentioned claims. Applicant respectfully disagrees with the Examiner's non-patentability conclusions. The discussion above has directly addressed some of those comments and the Examiner's other comments are deemed moot at this time in view of this response.

Applicant respectfully submits that the pending claims are in patentable form for at least the reasons stated above. Reexamination and reconsideration are respectfully requested. If, for

any reason, the application is not in condition for allowance, the Examiner is requested to telephone the undersigned to discuss the steps necessary to place the application into condition for allowance.

Respectfully submitted,

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Alan S. Raynes **March 3 , 2004**
(Date)